

REMARKS

Claims 1 – 11 are now pending in the application. Applicant thanks the Examiner for the indication that claims 6, 7 and 10 contain allowable subject matter. For the reasons discussed herein, applicant submits that the other claims are also allowable and the Examiner is respectfully requested to reconsider and withdraw the rejection(s) in view of the remarks contained herein.

OBJECTION TO THE DRAWINGS

The Examiner objected to the drawings, asserting that they fail to show a support shim being a corner shim having first and second leg sections at generally right angles to each other and inwardly extending top flanges having first and second sections at generally right angles to each other. Applicant respectfully traverses this objection and submits that the drawings do in fact show this feature(s). The Examiner is directed to Figure 2. As described in the application, Figure 2 shows a support shim 30 “formed as a corner section having first and second leg sections 32 generally at right angles to each other and an inwardly extending top flange 34 having first and second sections 36 at generally right angles to each other.” [Application, p. 5]

REJECTION UNDER 35 U.S.C. § 103

Claims 1 – 5, 8 – 9 and 11 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Tao (U.S. Pat. No. 6,410,981) in view of Best et al. (U.S. Pat. No. 3,561,107). Applicant respectfully traverses this rejection.

Tao is directed to a vented semiconductor device package. More specifically, Tao's semiconductor device package is formed by mounting a semiconductor chip 4 having solder bumps 8 on an isolated substrate 3 with the solder bumps 8 disposed between the top surface of the isolated substrate 3 and the bottom surface of semiconductor chip 4. A strengthening ring 2 is adhered to the isolated substrate 3 and a cap is adhered to the semiconductor chip 4 and strengthening ring 2. Solder balls 6 are adhered to the bottom surface of isolated substrate 3 for loading the packaged semiconductor device on the printed circuit board. [Tao, col. 3, line 64 – col. 4, line 14; col. 2, lines 3 - 5]

Best discloses a semiconductor process for joining a transistor chip to a printed circuit. A substrate 10 has a printed circuit having contact areas 18, 20 and 22 at the ends of conductive members 12, 14, 16. Contact areas 18, 20, 22 are arranged to correspond to similar metallic contact areas 24, 26 and 28 on a transistor chip 30. Solid conductive pillars 32, 34, 36 are attached to contact areas 24, 26, 28 of transistor chip 30.

The Examiner takes the position that Tao discloses every feature of claims 1 – 5, 8, 9 and 11 except for the use of solder columns, which the Examiner asserts are disclosed by Best et al. More specifically, the Examiner takes the position that Tao's isolated substrate 3 is a circuit board and that Tao's semiconductor chip 4 is an integrated circuit package having a substrate with an array of solder bumps 8 extending from a bottom surface of the substrate to the circuit board when the integrated circuit package is mounted on the circuit board.

Applicant respectfully disagrees. Applicant's invention is directed to supporting an integrated circuit package having solder columns on a circuit board so as to prevent compressive force on the solder columns. In contrast, Tao is directed

to a packaged semiconductor device and at best shows supporting a semiconductor chip 4 within the packaged semiconductor device. Tao's semiconductor chip 3 and isolated substrate 3 are both part of the part of Tao's packaged semiconductor device. Tao's solder bumps 8 are thus disposed within the packaged semiconductor device and connect the semiconductor chip 4 to the isolated substrate 3 which is part of Tao's packaged semiconductor device. Similarly, ring 2 extends between cap 1 and isolated substrate 3 of Tao's packaged semiconductor device and is part of the packaged semiconductor device. Ring 2 does not extend between cap 1 and the printed circuit board on which Tao's semiconductor device is mounted. In this regard, it is solder bumps 6 that extend between the Tao's packaged semiconductor device and the printed circuit board when Tao's packaged semiconductor device is mounted on the printed circuit board. [Tao, col. 2, lines 7 – 9; col. 4, lines 3 – 5] As can be seen from Tao's drawings (e.g., Figs. 1 and 3), ring 2 does not in anyway support solder bumps 6 against compression as it is wholly disposed above isolated substrate 3. Thus, Tao fails to disclose at least one support shim disposed between a portion of a lid that extends beyond the outer periphery of a substrate of an integrated circuit package and a portion of the circuit board to which the integrated circuit package is mounted to support a column grid array extending from the bottom surface of the substrate against compressive force, as required by claim 1. Best et al. similarly fails to disclose this, and the Examiner does not cite it as doing so, Applicant submits that claim 1 is thus allowable over the combination Tao and Best et al. Applicant also notes that there is no mention in Best et al. that conductive pillars 32, 34 and 36 are an array of solder columns. In fact, Best et al. describes conductive pillars 32, 34 and 36 as being made of copper, aluminum or the like.

Claim 8, the other independent claim, requires a support shim disposed at each corner of a column grid array integrated circuit package between a portion of a lid affixed to a substrate of the integrated circuit package that extends beyond the outer periphery of the substrate and a portion of the circuit board to which the column grid array is mounted to support the column grid array integrated circuit package against compressive force. As discussed, Tao's ring 2 does not extend between cap 1 and the circuit board to which Tao' packaged semiconductor device is mounted to support solder bumps 6 against compressive force, let along comprise a support shim at each corner of the column grid array substrate. As such, Tao fails to disclose this structure required by claim 8. Similarly, Best et al. fails to disclose such a structure. Applicant submits that claim 8 is thus allowable over the combination of Tao and Best et al.

Claims 2 – 7 and claims 9 – 11 depend directly or indirectly from claim 1 or 8 and are allowable for at least that reason.

CONCLUSION

It is believed that all of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider and withdraw all presently outstanding rejections. It is believed that a full and complete response has been made to the outstanding Office Action, and as such, the present application is in condition for allowance. Thus, prompt and favorable consideration of this amendment is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (248) 641-1600.

Respectfully submitted,

Dated: April 26, 2004

By: R.A. Fuller III
Roland A. Fuller III
Reg. No. 31,160

HARNESS, DICKEY & PIERCE, P.L.C.
P.O. Box 828
Bloomfield Hills, Michigan 48303
(248) 641-1600